Hall Ticket Number:

Code No. : 13248 S

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (C.S.E./AIML) III-Semester Supplementary Examinations, August-2022

Computer Architecture

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10× 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Define Control Word, Microinstruction, Micro routine	2	1	1	1,2
2.	What are the registers involved in fetching an instruction from memory to processor?	2	1	1	1,2
3.	What is an Interrupt? List the types of interrupts.	2	1	2	1,2
4.	Write the advantages and disadvantages of hardwired and micro programmed control unit?	2	1	2	1,2
5.	Differentiate I/O Mapped I/O and Memory Mapped I/O mechanisms?	2	1	3	1,2
6.	What is Cycle Stealing and Burst mode Transfers in DMA Controller?	2	1	3	1,2
7.	Why the access time of the cache memory islesser than the access time of the main memory?	2	2	4	1,2
8.	Determine the maximum size of the memory that can be used in a 32-bit addressable computer?	2	2	4	1,2
9.	What is Pipelining? What are the major issues in Pipelining	2	1	5	1,2
10.	What are Data Hazards? How to handle Data Hazards in software?	2	1	5	1,2
	Part-B (5×8 = 40 Marks)				
11. a)	What is an addressing mode? Explain various addressing modes with examples	4	2	1	1,2
b)	To evaluate the performance of a processor SPEC suite is used. One of the applications from the SPEC suite is selected and executed on both the reference computer and the test computer. If the running time on a reference computer is 60 seconds and 50 seconds on a test computer, what is the SPEC rating?	4	3	1	1,2,3
12. a)	Draw the Hardwired Control Unit Organization and explain the functionality of each block	4	2	2	1,2
b)	Evaluate the given expression (A=B) *(C+D) using one-address, two-address, three-address instruction formats	4	3	2	1,2,3
13. a)	What is an Interrupt Latency? How to reduce the interrupt latency?	4	2	3	1,2
b)	Consider a daisy-chain arrangement. Assume that after a device generates an interrupt request, it turns off that request as soon as it receives the interrupt acknowledge signal. Is it still necessary to disable interrupts in the processor before entering the interrupt service routine? Why?	4	3	3	1,2,3

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14. a)	Explain the cache mapping functions with examples	4	2	4	1,2
b)	A block-set-associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words. i) How many bits are there in a main memory address? ii) How many bits are there in each of the TAG, SET, and WORD fields?	4	3	4	1,2,3
15. a)	Explain the 4-stage pipeline instruction execution and Hardware Organization	4	2	5	1,2
b)	Assume that 20 percent of the dynamic count of the instructions executed on a computer are branch instructions. Delayed branching is used, with one delay slot. Estimate the gain in performance if the compiler is able to use 85 percent of the delay slots.	4	3	5	1,2,3
16. a)	How can we make use of index addressing mode for accessing the array elements?	4	2	1	1,2
b)	Write the control sequence for the instruction Add R4,R5,R6 for the three-bus organization.	4	3	2	1,2
17.	Answer any ***two*** of the following:				
a)	WhenMultiple I/O devices may be connected to the processor and the memory via a bus. Some or all of these devices may be capable of generating interrupt requests. I. How does the processor know which device has generated an interrupt? II. How does the processor know which interrupt service routine needs to be executed? III. When the processor is executing an interrupt service routine for one device, can other device interrupt the processor? IV. If two interrupt-requests are received simultaneously, then how to break the tie?	4	3	3	1,2,3
b)	In many computers the cache block size is in the range of 32 to 128 bytes.what would be the main advantages and disadvantages of making the size of cache blocks larger or smaller?	4	3	4	1,2,3
c)	Describe the features of Intel IA-64 family.	4	2	5	1,2

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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